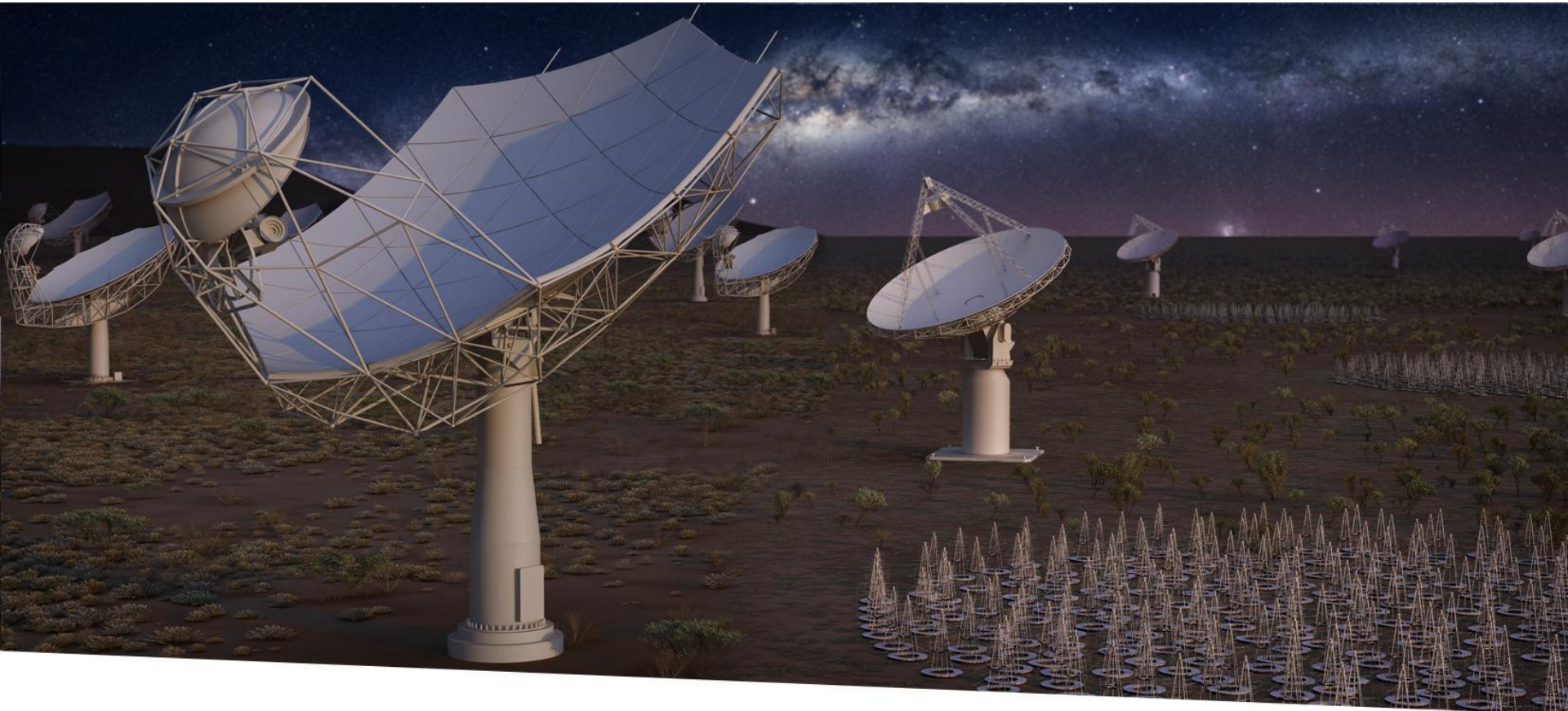


# WebJive Roadmap

A SKA perspective



**SQUARE KILOMETRE ARRAY**

Exploring the Universe with the world's largest radio telescope

**Giorgio Brajnik**  
**Interaction Design Solutions**

# Vision

- Important SKA deadline:  
**June 2021:** beginning of construction

Development of the WebJIVE **engineering web-based user interface tool** to a **sufficient level of maturity** such that it can be mandated for use in construction by all teams responsible for delivering software components based on the TANGO framework.

# Vision

For	Developers of TANGO systems, Operators using TANGO systems in the early years of operations, and SKA1 Commissioning teams
who	wish to create and/or configure custom web-based user interfaces to monitor and control TANGO systems
the	WebJIVE is a web-based configurable tool
that	allows users to create, modify and use their own UIs to TANGO systems
unlike	existing solutions (Taurus, EPICS EDM, ...)
our solution	is fully web-browser based and is based on modern Javascript frameworks
expected outcomes	WebJIVE is mature enough to be mandated for SKA construction teams to use as their <b>preferred UI tool for TANGO systems</b> , making it easy to create new interfaces which are <b>consistent</b> across the project; a set of UI and <b>HMI guidelines</b> to accompany the tool; and <b>digital assets</b> (logos, themes, ...) within WebJive that are compliant to those guidelines.
NFRs	Performance; Scalability; Usability; Reliability

# For example: performance

## High throughput:

- “each screen should handle an update rate of 1000 updated items/sec”
- “a screen should populate in less than 2sec”

## Low latency:

- “a command roundtrip time is less than 0.1sec”



# Roadmap - short term

## By the end of August:

- **Import/export dashboards**
- There are 3 **dashboards** for 10-15 devices within the correlator
  - they are **interconnected** (drill-down, wrap-up)
  - they are visually **appealing** (alignments, bg colors, boxes, images)
  - they are **information-dense**.
- **Improvements in user documentation** so that non SKA users can easily deploy WebJive, use it and extend it.

This is developed according the SKA Definition-of-Done and a Lean UX process.

# Roadmap - until June 2021

We are aiming at enabling users to develop complex monitoring and control UIs.

Like these ones:

# Examples of compelling UIs

s001-t-0 sb0006 s001-t-0.evla.nrao.edu Ant/St:1 BB:0/1 -- GUI s/w version: 29Oct2010 11:45AM

Screen Board Control FPGA GUI ErrorCounts Logging Misc

Name/IP: s001-t-0.evla.nrao.edu    BOARD    Temperature    Startup    Filter Gain    Clear All Errors

State: running    Serial #: 0x0006    CMIB    Voltage    CPU    Set Filters    Set Logical Configuration

Version: 20101119-1154    POWER    Temp/Volt Info    Registers    Crossbar    Refresh -- OFF sec: 10 Refresh

Main Logical Configuration ConfigQueue CRC BitStreamFiles LookupTables ConfigFiles OutputData TIC

Last Refresh Date & Time  
2011-01-26T23:03:01.886

Status & Control  
Interrupt Source timingFPGA  
CMIB Interrupt Enabled   
PCI Interrupt Enabled   
External Delay Models

DPO Ant/St:1 BB:0

DP1 Ant/St:1 BB:1

FORM    Input 8-Bit    Delay 0    Delay 1    WBC

Filter 0-17 (0x0b-0x1d)    VSI 0 (0x09)    MCB (0x00)    CFG (0x01)    Timing (0x06)    Output 0 (0x07)    Output 1 (0x08)

Filter 0-17 (0x1d-0x2e)    VSI 1 (0x0a)

2011-01-24 12:47:09 -- Restarted.  
01/24 12:47 widar - connected.  
01/24 12:47 widar - disconnected.  
01/26 15:03 vrcvis - connected.

up: 2d 4h 29m    Update

Lock State: \_\_\_\_\_

# Examples of compelling UIs

0f0 - Station Board 192.139.21.152 FILTER 0f0

**Main FPGA**

**Common**  
 Status: ok Last refresh: 2007-06-18T17:42:40.109  
 S/W Version: 0.1 FPGA D/V/R: 0 0 0  
 Config. File:  
 Bit Str. File:  
 Log Level: LOG\_WARNING  
 sysTickDelay: 0  
 Reset Inds/Counters  
 Register Set

**Status**  
 System Clock  
 SysTick Width  
 Pattern Error  
 Write to R0  
 Write to NE  
 Read from NE

**Register Access**  
 Refresh -- OFF  
 sec: 10  
 Once  
 Register: 0x00  
 Write + Read  
 Write Read

**TestGen**  
 Off  
 Random  
 Seed: 0x0000

**VCI**  
 Input band width (Hz): 204800000 Output band width (Hz): 128000000 Fbit:   
 Baseband offset (Hz): 200000000 Output band center (Hz): 640000000 Flip:   
 Input # bits: 3 Output # bits: 4 Mixer:   
 Input # bands: 1 Tone frequency (Hz): 0 MPEC:   
 Input band: 0 Delay module delay rate: 10.0 LSB:   
 Specify Models via GUI Tick Delay: 0  
 Delay: 0.0 Signal dominated input:  Setup  
 Delay rate: 0.0

**InOut**  
 StandBy mode  
 Input Port: 0  
 Input Mode:  4bit  8bit  
 Output:  0  1  
 AC balance  Bit 7 valid

**ClockEdge**  
 System Clock  +  -  
 Input Data  +  -

**Time Interval Counters**  
 dTick\_sTick 0  
 dTick 0  
 sTick 0  
 sTick\_dTick 0

**Format**  
 Select Data: stage1 Power: on 0 off 0  
 Valids: on 0 off 0  
 Select Clip: stage3 Clip Count: 0  
 RFI Detect Level: 0 RFI Inv. Stretch: 0 RFI Count: 0  
 Quantizer Scaling: 64 Quant. Power: 0  
 Quantizer # Bits: 4 Quant. Clip Cnt.: 0 Sideband Flipper  
 Quantized State: Auto 204 Quant.StateCnt.: 0  
 Load TEX File: Browse  
 Specify TEX Model via GUI Send TEX Model  Free running mode  
 TEX Phase: 0 TEX Valids: 0  
 TEX Phase Rate: 0 TEX Sums: cos 0 sin 0

**Delay1**  
 Divider: 0  Specify Delay Model via GUI  
 Demux Factor: 16  Free running mode  
 Delay Error Factor: 2048 Delay: 0  
 Fbit: VLBI delay mode Delay Rate: 0

**Stage1**  
 Product File: Browse  
 Output Divider: 0 Fractional Bits: 0  
 Invalid Stretch: 32 Filter Delay: 16  
 Scale Factor: 18 Number of Taps: 512

**Mixer**  
 Mixer Trig File: Browse  
 Use mixer  Specify Mixer Model via GUI Phase: 0  
 Use MPEC  Free running mode Phase Rate: 0

**Stage2**  
 Coefficient File: Browse  
 Output Divider: 12 Calculation Divider: 12  
 Invalid Stretch: 512 Filter Delay: 256  
 Scale Factor: 128 Number of Taps: 512

**Stage3**  
 Coefficient File: Browse  
 Output Divider: 12 Calculation Divider: 0  
 Invalid Stretch: 512 Filter Delay: 256  
 Scale Factor: 128 Number of Taps: 512

**Stage4**  
 Coefficient File: Browse  
 Output Divider: 12 Calculation Divider: 12  
 Invalid Stretch: 512 Filter Delay: 256  
 Scale Factor: 128 Number of Taps: 512

**Input Crossbar**  

FIR32[00]	0	FIR32[08]	8
FIR32[01]	1	FIR32[09]	9
FIR32[02]	2	FIR32[10]	10
FIR32[03]	3	FIR32[11]	11
FIR32[04]	4	FIR32[12]	12
FIR32[05]	5	FIR32[13]	13
FIR32[06]	6	FIR32[14]	14
FIR32[07]	7	FIR32[15]	15

**Delay2**  
 Output: 0  
 VSI: 0  
 Timing: 0

**CRC Mode**  
 Mode: auto  
 Input:  
 Output:  
 ForceErr: No 0 1 2 3

**CRC Errors**  
 Data Input 0  
 Data Input 1  
 Data Output 0  
 Data Output 1  
 OUTPUT  
 TIMING  
 VSI



# Roadmap - until June 2021

- conditional styles (fonts, colors based on values)
- grouping/ungrouping of items
- error handling and notifications
- configurable themes, logos
- improved usability of editor
- svg-based interactive synoptics
- tabs in dashboards
- architectural changes:
  - features can be toggled
  - plugins for widgets
  
- support for the Tango community:
  - establish an effective user feedback channel

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## Thank you for your attention!

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